Printed, Flexible, Organic Nano-Floating-Gate Memory: Effects of Metal Nanoparticles and Blocking Dielectrics on Memory Characteristics

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The effects of using a blocking dielectric layer and metal nanoparticles (NPs) as charge-trapping sites on the characteristics of organic nano-floating-gate memory (NFGM) devices are investigated. High-performance NFGM devices are fabricated using the n-type polymer semiconductor, poly{[*N*,*N*′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5′-(2,2′-bithiophene)} (P(NDI2OD-T2)), and various metal NPs. These NPs are embedded within bilayers of various polymer dielectrics (polystyrene (PS)/poly(4-vinyl phenol) (PVP) and PS/poly(methyl methacrylate) (PMMA)). The P(NDI2OD-T2) organic field-effect transistor (OFET)-based NFGM devices exhibit high electron mobilities (0.4–0.5 $cm^2 V^{-1} s^{-1}$) and reliable non-volatile memory characteristics, which include a wide memory window (≈52 V), a high on/off-current ratio ($I_{on}/I_{off} \approx 10^5$), and a long extrapolated retention time (>10^7 s), depending on the choice of the blocking dielectric (PVP or PMMA) and the metal (Au, Ag, Cu, or Al) NPs. The best memory characteristics are achieved in the ones fabricated using PMMA and Au or Ag NPs. The NFGM devices with PMMA and spatially well-distributed Cu NPs show quasi-permanent retention characteristics. An inkjet-printed flexible P(NDI2OD-T2) 256-bit transistor memory array (16 × 16 transistors) with Au-NPs on a polyethylene naphthalate substrate is also fabricated. These memory devices in array exhibit a high I_{on}/I_{off} (≈$10^{4 \pm 0.85}$), wide memory window (≈43.5 V ± 8.3 V), and a high degree of reliability.

1. Introduction

Printed organic electronic and optoelectronic devices such as organic light-emitting diodes (OLEDs), organic photovoltaics (OPVs), and organic field-effect transistors (OFETs) have the potential to be used in a number of novel consumer applications as these devices, which can have large areas and are light-weight, can be fabricated in freeform shapes on flexible substrates at extremely low costs.[1–3] Most of these electronic and optoelectronic devices inevitably involve functions that require memories that have discrete ON and OFF states, high switching speeds, the ability to retain their states for relatively long periods (i.e., they are non-volatile in nature), and that can be programmed and erased preferably by electrical signals.[2] Although state-of-the-art technologies for commonly used memories, which are mostly inorganic-based flash ones, have progressed rapidly to the point where high-capacity solid-state drives are being broadly commercialized at reasonably low prices,[4] there is still a need for an immortal, universal memory that can fulfill the soaring demand for data storage. Moreover, currently available inorganic memories are not compatible with flexible substrates, and therefore, new approaches are needed to fabricate a data storage suitable for the printed flexible electronic devices currently under development.[3] With this in mind, organic memories are increasingly being considered as promising candidates for such applications as these memories are mechanically flexible and can be processed at low temperatures using solutions.

Organic flash memories have the similar geometry as OFETs. They differ in that in organic flash memories, a charge-storing medium such as metallic or semiconductive nanoparticles,[5,6] a thin layer of metal, or a layer of a chargeable polymer, i.e., electrets,[7,8] is incorporated in the gate dielectric layer as a floating gate. Although conventional floating-gate-based memories are being widely used in portable electronic devices, they are considered to have reached their limits with respect to their dimensions, further efforts to scale them down result in current leakages, owing to tunneling though the thin dielectric layers.[9] As a solution to this problem, discrete nanocrystal memories, i.e.,

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nano-floating-gate memory (NFGM) devices have been developed, which can function as universal memories owing to their high speed of operation, superior reliability, and capacity for being programmed at multiple levels and for being scaled down.[10] Organic NFGM devices have mainly been fabricated using metallic nanoparticles (NPs) (most commonly Au NPs) that have been thermally deposited or chemically assembled, such as those by block-copolymer structures[11,12] and organic nanocomposites such as [6,6]-phenyl-C(61) butyric acid methyl ester.[8] These metallic NPs are embedded within a polymer dielectric matrix.

The operation mechanism of organic NFGMs is very similar to that of conventional Si-based flash memory devices. When a suitably strong external electric field is applied to the gate electrode of the memory device, mobile charge carriers are injected into and trapped within the floating gate, which is surrounded by a layer of tunneling and blocking dielectric that has been placed between the gate electrode and the semiconducting layer. This is then followed by gate field modulation, which increases or decreases of the threshold voltage (V_{Th}), depending on the polarity of the charge stored in the floating gate.[11] Currently, most organic NFGMs exhibit relatively poor device characteristics along with markedly shorter retention times and slower switching speeds and require relatively higher operating biases than those in the case of their inorganic counterparts and cross-point-type organic memories.[13] Therefore, for the development of high-performance NFGM devices, it is essential that these devices be optimized. This is only possible by understanding the exact mechanism underlying their operation and carefully selecting the key materials, in particular the dielectric and metal whose nanoparticles are to be used in the devices.

In this study, we investigated the effects of metallic NPs and gate dielectrics on the characteristics of organic NFGM devices fabricated using the high-performance n-type (potentially ambipolar) polymer semiconductor poly{[*N*,*N*′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5′-(2,2′-bithiophene)} (P(NDI2OD-T2) (Polyera ActivInk N2200)). The use of NPs of various metals, including those of Au, Ag, Cu, and Al, as a floating gate was investigated by inserting the NPs between the bilayers of various polymer dielectrics (polystyrene (PS)/poly(4-vinyl phenol) (PVP) or PS/poly(methyl methacrylate) (PMMA)). Top-gate/bottom-contact (TG/BC) P(NDI2OD-T2)-based OFETs fabricated on glass substrates using these NPs exhibited a high electron mobility (of up to 0.4 $cm^2 V^{-1} s^{-1}$) and reliable memory characteristics, including a wide memory window (≈52 V), high ON/OFF-current ratio (I_{on}/I_{off}) (≈10^5), and long extrapolated retention time (>10^7 s). The characteristics of the P(NDI2OD-T2)-based NFGM devices depended strongly on the choice of the blocking dielectric (PVP or PMMA) as well as that of the metal (Au, Ag, Cu, or Al) whose NPs were used. Large memory window and high I_{on}/I_{off} characteristics were achieved by using PMMA as the controlling dielectric and Au or Ag NPs as the nano-floating gate. This was because these choices resulted in a relatively long charge-relaxation time and high surface density of the NPs. An array of 256-bit (16 × 16 transistors) inkjet-printed organic NFGM devices was also fabricated successfully on a flexible polyethylene naphthalate (PEN) substrate. These memory devices exhibited a high I_{on}/I_{off} (of ≈$10^{4 \pm 0.85}$; standard deviation <21%), a wide memory window (≈43.5 V ± 8.3 V; standard deviation <19%), device yield of more than 99%, and a high degree of reliability, with the values being measured using over 100 such devices.

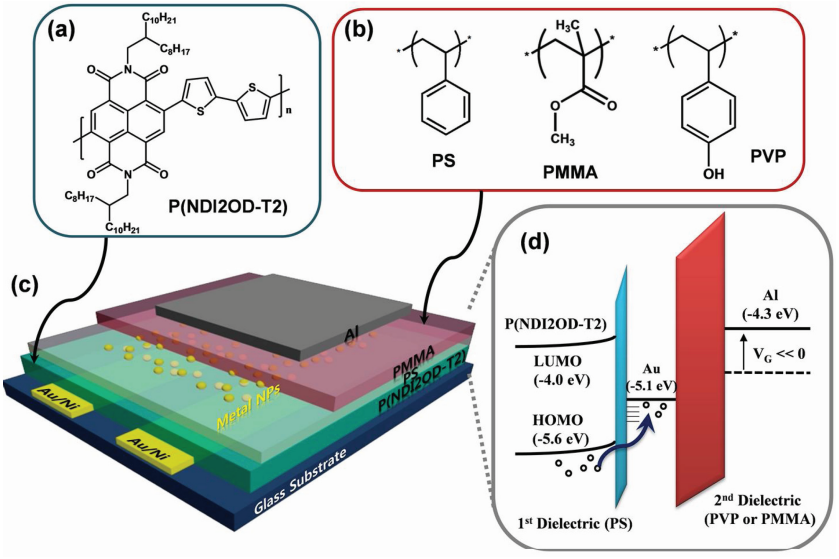

Figure 1. Molecular structures of a) the polymer semiconductor P(NDI2OD-T2) and b) the polymer dielectric PS, PMMA and PVP. c) Structure of an organic NFGM device based on TG/BC OFET geometry. d) Schematic illustration of the operating mechanism of the organic NFGM device shown in (c).

2. Results and Discussion

2.1. Characteristics of the OFET Devices

Figure 1 shows a schematic of an organic NFGM device based on the TG/BC OFET geometry and the chemical structures of the n-type polymer semiconductor (P(NDI2OD-T2)) and the various gate dielectrics (PS, PVP, and PMMA) used. P(NDI2OD-T2) is a recently developed high-performance n-channel semiconducting polymer that has a high electron mobility of 0.1–0.84 $cm^2 V^{-1} s^{-1}$, high solubility in common organic solvents, and good stability in air.[14,15] Moreover, P(NDI2OD-T2) exhibits seemingly ambipolar charge transportation characteristics because its polymer backbone has alternately placed electron-donor and electron-acceptor moieties for the efficient transport of holes and electrons, respectively. Owing to its seemingly ambipolar characteristics, P(NDI2OD-T2) is preferable for fabricating charge-trapping organic memories, since it contains electrons and holes in large enough quantities such that it is easy to efficiently program and erase the OFET memories based on it.[16] The TG/BC OFET structure was chosen

because it results in a relatively low contact resistance,[17] as well as higher stability in air owing to self-encapsulation by the overlaid gate dielectric layer and gate electrode. However, the biggest advantage of using the TG/BC geometry is the ease with which it is possible to achieve ambipolar characteristics, which can be achieved by efficiently injecting electrons and holes from the BC Au electrode and a proper selection of the gate dielectrics.[18]

A low-k/high-k (k being the permittivity) polymer dielectric bilayer, i.e., PS (relative permittivity, ε_r = 2.6)/PVP (ε_r = 4.7) or PS/PMMA (ε_r = 3.5) was used to increase the carrier concentration at the semiconductor-dielectric interface and to induce efficient charge injection from the ambipolar semiconductor into the metallic NFGs.[11,19] The low-k dielectric PS, whose layer was relatively thin (≈40 nm), was used as a tunneling gate dielectric for injecting charge from the semiconductor into the NFGs. It was also used as a passivation layer for the semiconductor active layer from metallic NPs, which penetrated into the active channel during the thermal evaporation process. We would like to point out that a relatively high electric field is loaded at the first low-k dielectric layer because the magnitude of the electric field applied to the bilayer of the low-k/high-k dielectrics is inversely proportional to the ε_r of the insulator,[20] and this enables the efficient transfer of charge from the semiconductor to the NFGs. PVP and PMMA, whose layers were relatively thicker at ≈220 nm and ≈260 nm, respectively, were used as blocking dielectrics to minimize the gate leakage current and to store the charge trapped in the NFGs for as long as possible. As noted previously, in this study, NPs of various metals such as Au, Ag, Cu, and Al, were incorporated between the bilayers of gate dielectrics, so that the trapping sites within them could store the charge injected into the NPs.

Figure 2 shows the typical transfer characteristics of the TG/BC P(NDI2OD-T2)-based OFETs fabricated using different combinations of the dielectrics (W/L = 1.0 mm/10 μm), including a single polymer layer (PS, PVP, or PMMA) (Figure 2a,b) and a bilayer (PS/PVP or PS/PMMA) (Figure 2c,d). The basic device parameters, such as the saturation mobility (μ_{sat}), V_{Th}, I_{on}/I_{off}, and subthreshold swing (SS) are listed in **Table 1**. The value of μ_{sat} was obtained by gradual channel approximation in the saturation region (at a high drain voltage, V_d, of 60 V).[21] As can be seen in Figure 2a,b, the OFETs fabricated using P(NDI2OD-T2) and the PS and PMMA dielectrics, respectively, showed excellent n-channel characteristics (μ_{sat} = ~0.4 cm^2 V^{-1} s^{-1}), while the P(NDI2OD-T2) device with PVP as the dielectric exhibited

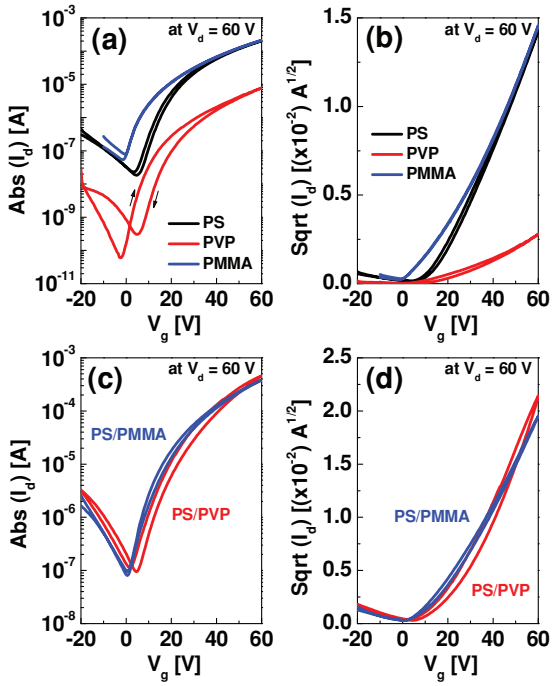

Figure 2. Transfer characteristics at the saturation region (V_d = 60 V) of top-gate P(NDI2OD-T2)-based OFETs fabricated using the various polymer gate dielectrics: a,b) using single layers of the polymer gate dielectrics PS, PVP, and PMMA and c,d) using the dielectric bilayers PS/PVP and PS/PMMA. Panels (a,c) show Abs(I_d) vs. V_g and (b,d) show sqrt(I_d) vs. V_g.

a relatively low μ_{sat} value, of ≈0.02 cm^2 V^{-1} s^{-1}. This was mainly due to the trapping of mobile electrons by the hydroxyl groups (–OH) in the PVP layer.[22] When a thin PS layer was inserted between the P(NDI2OD-T2) and PVP layers, the value of μ_{sat} recovered to a level similar to those of the original PS-dielectric-based device owing to the complete separation of the active channel from the hydroxyl groups in PVP. The devices with the dielectric bilayer of PS/PVP exhibited a higher drain current (I_d) at the same bias and for the same bilayer thickness than did the PS/PMMA devices since the PS/PVP bilayer exhibited a higher dielectric capacitance and a stronger electric field was generated at the interface between the semiconductor and PS layers (PVP has a higher ε_r of 4.7 than does PMMA, whose ε_r is 3.5). Moreover, all of the TG/BC P(NDI2OD-T2) OFETs used

Table 1. Fundamental parameters of the P(NDI2OD-T2)-based OFETs fabricated using the various gate dielectric layers: channel width/length = 1.0 mm/10 μm.

Parameters	PS	PVP	PMMA	PS/PVP	PS/PMMA
Dielectric constant	2.6	4.7	3.5	2.6/4.7	2.6/3.5
Thickness [nm]	520	480	460	40/210	40/190
Capacitance [nF/cm^2]	4.4	9.2	6.7	14.7	12.7
Electron mobility [cm^2/V s]	0.41 ± 0.1	0.02 ± 0.001	0.42 ± 0.1	0.48 ± 0.05	0.42 ± 0.06
V_{Th} [V]	17.5 ± 0.6	4.5 ± 1.1	15.4 ± 0.8	18.8 ± 3.08	15.2 ± 0.87
I_{on}/I_{off}	≈10^4	≈10^4	≈10^3	≈10^4	≈10^3
SS [V/dec.]	4.9 ± 0.2	6.4 ± 0.7	5.0 ± 0.4	7.7 ± 0.8	5.7 ± 0.7

in this study exhibited ambipolar characteristics at a high V_d value of 60 V although their hole mobilities were relatively low at approximately 10^{-3} cm^2 V^{-1} s^{-1}.

2.2. Effect of the Dielectrics on the Memory Characteristics

As can be seen in **Figure 3**a, no significant bias hysteresis was observed in OFETs that had the metal-NPs-free PS/PMMA and PS/PVP dielectric bilayers. This was attributed to the poor charge-trapping characteristics of PS. In addition, no insignificant charge accumulation was observed at the interface of the polymer bilayer because the amount of current leaking through the layer of PMMA or PVP, which acted as blocking layers, was comparable to the charging current injected from the semiconductor into the PS layer or the interface.[11] It should be pointed out that the barrier to the injection of charge from the organic semiconductor into the first polymer dielectric layer (i.e., that of PS) is obviously higher than that between the first and second polymer dielectrics (PMMA or PVP).[11]

On the other hand, the P(NDI2OD-T2) OFETs with the Au NPs (in a 1.0 nm thick layer at the time of deposition) embedded at the interface between the PS and PMMA dielectric layers exhibited a large bias hysteresis. That is to say, there were large shifts in the V_{Th} values between the forward and reverse V_g scans (Figure 3b). During the V_g sweep from −50 V to +50 V, the initial transfer curves were shifted in the negative direction by ≈0.9 V, but did not return to their original state when a V_g of 50 V was applied again. A reversible bias hysteresis was observed only on the application of $V_g \geq \pm 60$ V. This prominent hysteresis loops reveal that these memory characteristics resulted from the trapping of charge in the Au NPs, and that

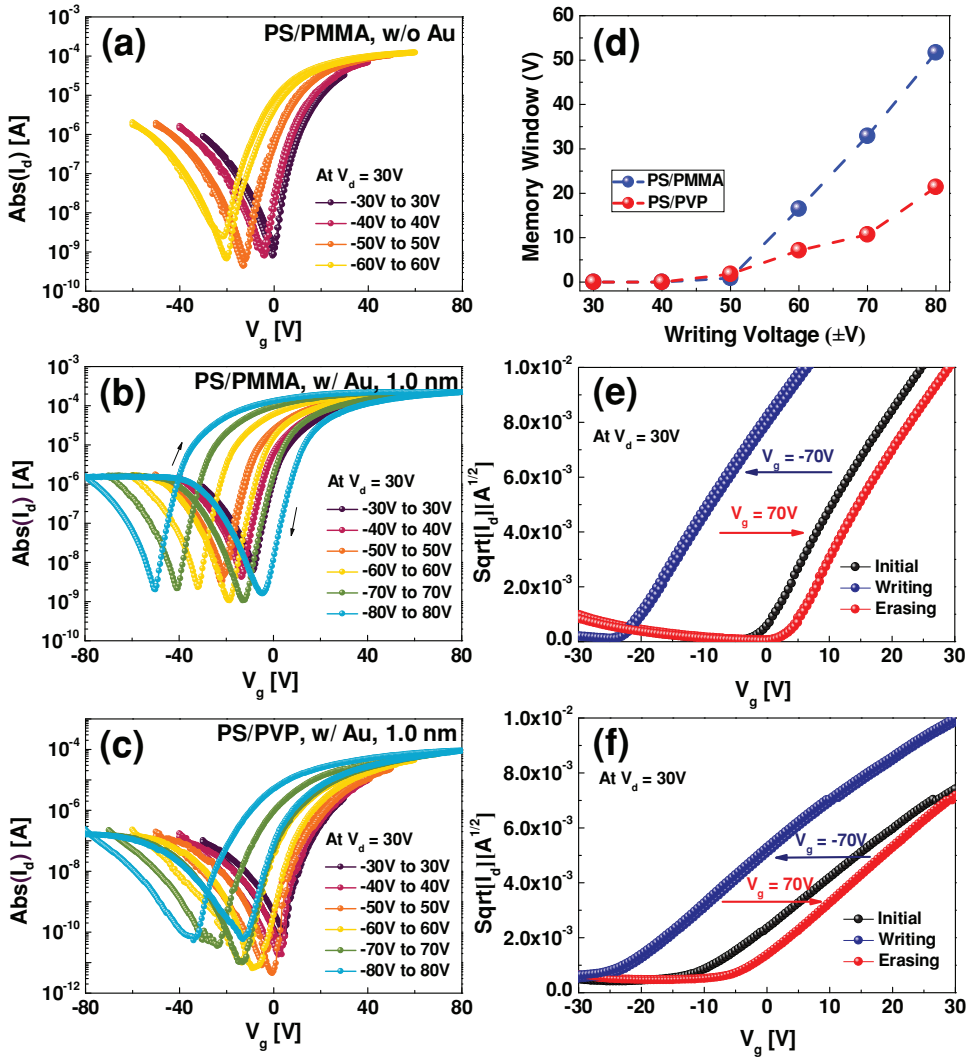

Figure 3. Memory characteristics of the P(NDI2OD-T2)-based OFETs fabricated using the PS/PVP or PS/PMMA dielectric bilayers. The bias hysteresis and memory window as determined at $V_d = 30$ V during the application of V_g sweep ranging from ±30 V to ± 80 V: a) in the devices fabricated using PS/PMMA without Au NPs, b) using PS/PMMA and Au NPs, and c) using PS/PVP and Au NPs. d) Change in the memory windows owing to an increase in the value of V_g applied to PS/PMMA and PS/PVP dielectric bilayers having Au NPs embedded within them. Results of the sequential writing and erasing operations (reversible V_{Th} shifts) performed by applying of V_g −70 V and +70 V at $V_d = 30$ V for the writing and erasing processes, respectively. e) Devices with the PS/PMMA and (f) the PS/PVP dielectric bilayers with the Au NPs.

the amount of stored charge determines the induced memory window, which is given by the following equation:

$$\text{Memory window} = \Delta V_{Th} = -Q/C_i \quad (1)$$

where the Q and C_i are the charge stored in the NFGs and the capacitance of the gate dielectrics, respectively. Once the NFGs had been charged, a higher number of charge carriers accumulate in the transistor channel than is the case in normal NFGs-lacking OFETs at the same gate electric field, owing to the electrostatic potential of the trapped charge.[23] During the reverse V_g sweep, the NFGs are discharged again by the charge carriers having the opposite polarity, and the shifted transfer plot moves back to its initial position. The memory windows of the devices depended strongly on the electric field applied at the gate electrode. This was because of the number of charge carriers injected into and trapped within the metallic NPs. As shown in Figure 3d, the memory windows of the organic NFGMs fabricated using the dielectrics PS/PMMA and the Au NPs (1.0 nm thick) increased markedly for values of V_g greater than ±50 V and reached values of up to ≈52 V after the application of a V_g of ±80 V.

Even though the P(NDI2OD-T2)-based NFGM devices fabricated using the Au-NPs- embedded PS/PVP dielectric bilayer exhibited distinct bias hysteresis, they showed narrower memory windows than those of the devices based on the PS/PMMA dielectric bilayer, as shown in Figure 3c,d. The memory windows for both type of devices increased by an amount proportional to the applied V_g, but the increase in the memory windows in the case of PS/PVP devices reached a maximum of 20 V and did not increase further even after the application of a higher V_g of ±80 V. Figure 3e,f show the reversible shifts in the transfer plots of the organic NFGMs after the application of a pulse-like (<1 s) V_g of −70 V and +70 V at a V_d of 0 V to induce discrete drain current levels for the ON and OFF states, respectively. These results also confirmed that the memory devices with the dielectric bilayer of PS/PMMA showed wider memory windows than those of the devices with the PS/PVP bilayer. The relatively large degree of hysteresis noticed in the case of the PS/PMMA devices can be attributed mainly to the charge relaxation time (t_{dr}) of the PMMA films being longer than that of the PVP films, with t_{dr} being determined by the ε_r and conductivity (σ) of the dielectric materials,[24] as shown by the following Equation (2):

$$t_{dr} = (\varepsilon_r \varepsilon_o)/\sigma \quad (2)$$

where ε_o is the permittivity in vacuum. In general, dielectrics films that are polar and hydrophilic to a higher degree, such as those of PVP, have surface and bulk conductivities (σ) that are a few orders of magnitude higher than those of hydrophobic and nonpolar polymer films, because the polar dielectrics have a number of contributory electric conduction pathways, such as those resulting from the presence of residual ions, dipoles, and adsorbed moisture with them.[25] The poor retention characteristics of the organic NFGMs with the dielectric bilayer of PS/PVP are mainly caused by a rapid dissipation of the stored charge through the leakage pathways present in the PVP film, which has a relatively higher conductivity. **Figure 4** displays the retention characteristics of the organic NFGMs with the

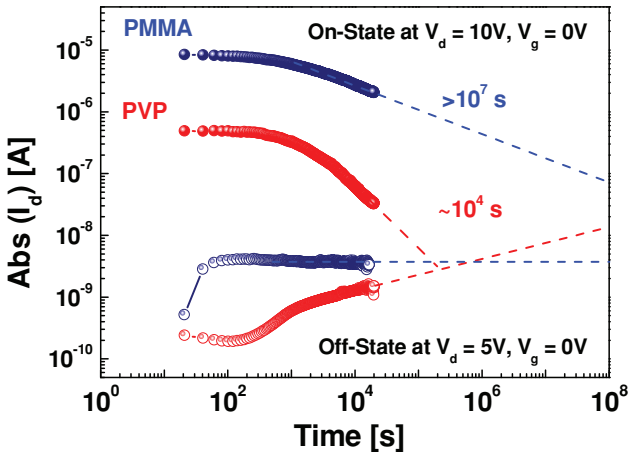

Figure 4. Memory retention characteristics at the ON states (filled circles) and the OFF states (opened circles) of the organic NFGM devices fabricated using the PS/PMMA (blue circles) and PS/PVP (red circles) dielectric bilayers that have Au NPs (1.0 nm thick). The currents at ON and OFF states were measured over a time interval of 20 s at V_d = +10 V and V_d = +5 V, respectively, at V_g = 0 V. The charge retention time was estimated by the extrapolation of each ON- and OFF-state plot.

Au-NPs-(1.0 nm thick)-embedded PS/PMMA and PS/PVP dielectrics layers. The current values for the ON states (at V_d = 10 V and V_g = 0 V) and OFF states (at V_d = 5 V and V_g = 0 V) were read over a time interval of 20 s after the application of V_g = –80 V and +80 V for programming and erasing the memory devices, respectively. The values of retention time of the NFGM devices with the bilayers of the PS/PMMA and PS/PVP dielectrics were determined to be more than 10^7 s and ≈10^4 s, respectively, by extrapolating the I_d plots at the ON and OFF states. To the best of our knowledge, the retention testing reported here indicates that the better or comparable retention characteristics compared to the previously reported results from other organic NFGM devices.[11,28,36]

2.3. Effect of the Metallic NPs on the Memory Characteristics

The metallic NPs contribute significantly to the memory characteristics of the NFGM devices. Au NPs were primarily used in devices fabricated in this study, owing to their high chemical stability, the ease with which they can be formed in a quite uniform manner using thermal evaporation and the small energy perturbation due to carrier confinement.[9,26] However, a variety of metallic NPs such as those of Ag, Cu, and Al should also be studied in order to obtain further optimized NFGMs.[27,28] To analyze and compare the memory characteristics of the P(NDI2OD-T2)-based OFETs fabricated using various metallic NPs, the transfer plots of the different OFETs were obtained for the same bias conditions (i.e., the application of a V_g ranging from –80 V to +80 V at a V_d = 30 V) while using the same bilayer of polymer dielectrics (PS/PMMA). **Figure 5**a–d show transmission electron microscopy (TEM) images of 1.0 nm-thick thermally deposited layers of Au (Figure 5a), Ag (Figure 5b), Cu (Figure 5c), and Al (Figure 5d) on the first dielectric layer, i.e., PS. The rate of thermal deposition and thicknesses of the

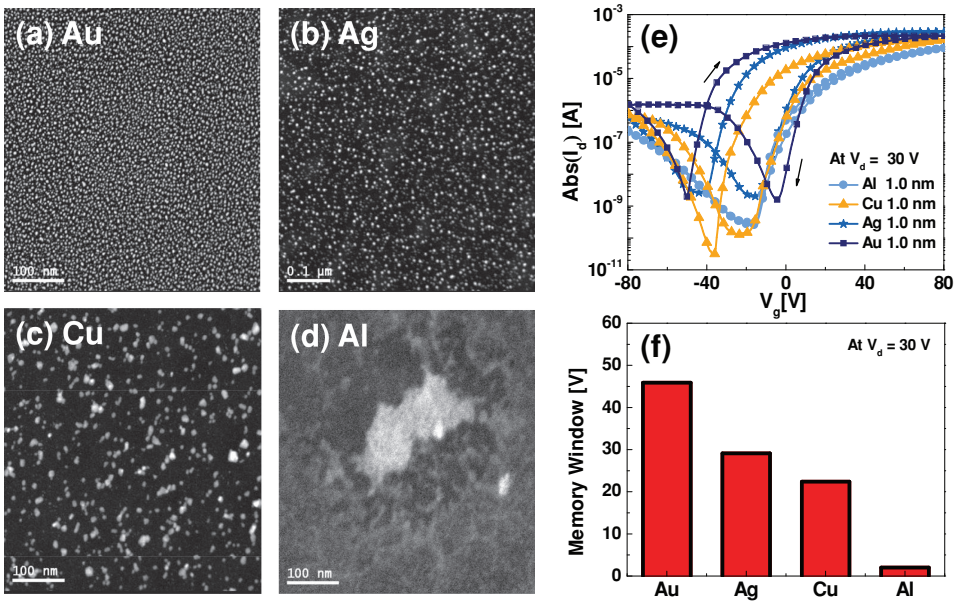

Figure 5. a–d) TEM images of the various thermally deposited metallic NPs (1.0 nm thick deposited): a) Au, b) Ag, c) Cu, and d) Al. e) Memory hysteresis loops and f) corresponding memory windows of the transfer plots, Abs(I_d) vs. V_g at V_d = 30 V, for the OFETs fabricated with various metallic NPs, i.e., those of Au, Ag, Cu and Al.

layers of all the metallic NPs were the same at ≈0.1 Ås^{-1} and 1.0 nm, respectively. It can be seen from the TEM images that Au and Ag NPs were uniformly distributed on the PS films, with the average sizes of the NPs being ≈4.6 nm for Au and ≈6.8 nm for Ag. In contrast, as shown in Figure 5c,d, the Cu and Al NPs had bigger average sizes: ≈13 nm in the case of Cu and ≈200 nm in the case of Al. In addition, the NPs of these metals were distributed randomly in a nonuniform fashion. It is likely that these different sizes and spatial distributions of the various metallic NPs contributed to the properties, such as the memory windows and retention time, of the various NFGM devices being different. As shown in Figure 5e,f, the memory windows increased in proportion to the surface number density of the NPs. Thus, the Au-NPs-containing devices, which had the highest density of NPs (≈3.0×10^{12} cm^{-2}), showed the widest memory window, of ≈52 V. In contrast, the devices with Al NPs showed very narrow memory windows because most of the thermally deposited Al formed aggregated particles, with the diameter of the particles being relatively large at ≈200 nm, leading to the number density of the Al NPs on the surface of the PS layer being low, as summarized in **Table 2**.

The process of embedding the metallic NPs in the PS substrate by thermal evaporation comprised the following steps: i) the mass transport of the evaporated metal from the source to the substrate surface, ii) the condensation and nucleation of the metal atoms on the substrate surface, iii) the diffusion of the metallic NPs through the surface, and iv) a further ripening process that takes place in the bulk dielectric.[29,30] Thus, the size and distribution (both horizontally and vertically) of the deposited metallic NPs is determined mainly by the atomic surface mobility, chemical reactivity, and density of the metals.[31,32] Since a decline in the deposition rate typically decreases the

Table 2. Fundamental parameters of the organic NFGMs fabricated using various metallic NPs (channel width/length = 1.0 mm/10 μm).

Parameter	Au	Ag	Cu	Al
Work function [eV]	5.10 – 5.47	4.52–4.74	4.53–5.10	4.06–4.26
Thickness of deposited layer [nm]	1.0	1.0	1.0	1.0
Average NP size [nm]	4.6	6.8	13	≈200
NP surface density [cm^{-2}]	3.0×10^{12}	1.5×10^{12}	1.0×10^{12}	NA
Memory window [V] (applied V_g)	0.9 (±50 V)	0 (±50 V)	0 (±50 V)	0 (±50 V)
	16.5 (±60 V)	2.2 (±60 V)	0 (±60 V)	0 (±60 V)
	32.9 (±70 V)	11.7 (±70 V)	9.1 (±70 V)	0 (±70 V)
	51.7 (±80 V)	29.1 (±80 V)	22.4 (±80 V)	2 (±80 V)
Charge stored per NP (at V_g = ±80 V)	1.3	4.5	13.8	NA
Extrapolated retention time [s]	≈10^7	>10^7	>10^8	NA

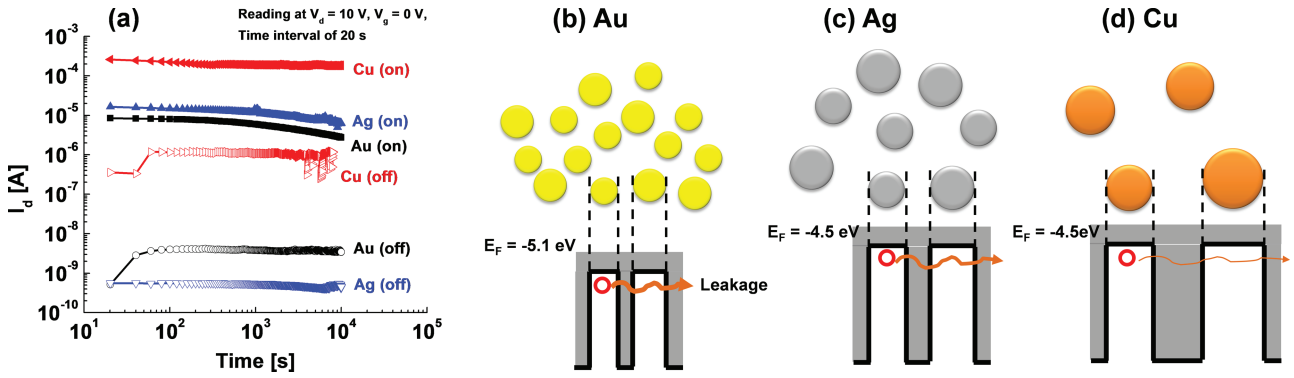

Figure 6. a) Memory retention characteristics during the ON state (filled circles) and the OFF state (opened circles) of the organic NFGM devices fabricated using the PS/PMMA bilayer and various metallic NPs: Au (black), Ag (blue), and Cu (red). The currents for the ON and OFF states were measured over a time interval of 20 s at V_d = +10 V and V_d = +5 V, respectively, at V_g = 0 V. b–d) Schematic illustration of the charge-retention characteristics of the various organic NFGMs with the various metallic NPs: b) Au, c) Ag, and d) Cu.

surface mobility of the evaporated metal ions, the formation of smaller-sized metallic NPs occurs preferentially.[33] As the size of the particles decreases, their surface density increases, and this results in the memory windows of the corresponding NFGM devices being wider. However, the charge trapped within the metallic NPs exhibiting high surface density becomes relatively unstable, and dissipates easily through the neighboring NPs, which act as leakage pathways. Thus, these metallic NPs may not be suitable for use when long retention times are desirable. **Figure 6**a shows a comparison of the retention characteristics for the ON- and OFF-state currents in the case of NFGM devices with Au, Ag, and Cu NPs. The memory device with Al NPs has not been included since its memory window was extremely narrow. After the application of the programming (V_g = –80 V and V_d = 0 V) and erasing (V_g = +80 V and V_d = 0 V) biases, the values of I_d for the ON and OFF states were measured at V_g = 0 V and V_d = 10 V with the measurement interval being 20 s. The initial I_{on}/I_{off} of the devices with the embedded Au, Ag, and Cu NPs were higher than ≈10^4, ≈10^3, and ≈10^2, respectively. All the data stored in the various organic NFGMs fabricated using Au, Ag, and Cu NPs were retained for periods longer than 10^7 s. In particular, in the case of the Cu-NPs-based devices, the values of the ON- and OFF-state currents remained almost similar to those at the origin, leading to quasi-permanent retention. On the other hand, the Au-NPs- and Ag-NPs-based devices showed a slight decrease in the ON-state current, with the Ag-NPs-based devices exhibiting better retention characteristics than those of the Au-NPs-based devices. It was obvious that the retention characteristics of the NGFM devices were affected by size, shape, and spatial distribution of the metallic NPs. NPs present in a high surface number density can store a higher amount of charge. However, the charge stored in such NPs leaks easily through the neighboring NPs. Although the high energy barrier height of the metal NPs surrounded by dielectric medium can alleviate the charge transport between the NPs, the charge stored in the NPs could still directly tunnel through the very thin layer of dielectric and/or through other leakage pathways, such as those provided by ions and dipoles.[34] On the basis of these factors, the quasi-permanent retention of charge seen in the case of Cu-NPs-based NGFM devices can be said to be mainly due to the sparse distribution of the NPs, which results in the lower leakage through the surrounding dielectric, making the devices suitable for use as nonvolatile charge storage media.

The hysteresis loops observed in the memory devices were also significantly influenced by the thicknesses of the deposited layers of Au NPs because of the difference in the charge-storing capacities of the various layers, as shown in **Figure 7**a,b. As can be seen from Equation (1), the memory window is determined by the charge stored in the NFGs. Notably, the shift in V_{Th} can be systematically controlled by changing the size, spatial distribution, and surface density of the NFGs. The average size (or surface number density) of the Au NPs was modified from 4.0 nm (6.2×10^{11} cm^{-2}) to 5.2 nm (1.8×10^{12} cm^{-2}) by changing the thickness of the deposited layer of Au from 0.5 nm to 1.5 nm, respectively. Correspondingly, the number of charge-trapping sites provided by the Au NPs also increased in proportion to the thickness of the deposited Au layer. Thus, a high enough thickness is preferable as it will result in more trapping sites being available, resulting in a wider memory window.[31] As shown in **Figure 8**a, the memory window increased markedly, from ≈10 V to ≈30 V, when the thickness of the deposited layer of Au was increased from 0.5 nm to 1.5 nm, respectively. However, if the layer of the NPs is too thick to form a continuous metal film, i.e., ≥2.0 nm, it can easily cause an electrical short circuit to occur owing to the resulting increase in the leakage current, thus negating the advantages of using discrete NFGs. In addition, the deposition rate also influences the formation of the NPs significantly. Figure 8c shows the transfer plots of various P(NDI2OD-T2)-based OFETs having embedded 1.0 nm-thick layers of Au NPs, which were formed using deposition rates of 0.1 Å s^{-1} or 0.2 Å s^{-1}. It can be seen that the memory windows of the NFGM devices decreased in the case of the higher deposition rate. As can be seen in Figure 8a,b, when the deposition rate is slow, uniform and smaller-sized (thus having a higher surface density) NPs were formed, making the corresponding devices more suitable for memory operations (see Figure 8c) as opposed to the memory devices fabricated using layers of NPs of the same metal that were deposited at a higher rate.

Cycling endurance tests performed on electrically reprogrammable non-volatile memories through a series of writing/

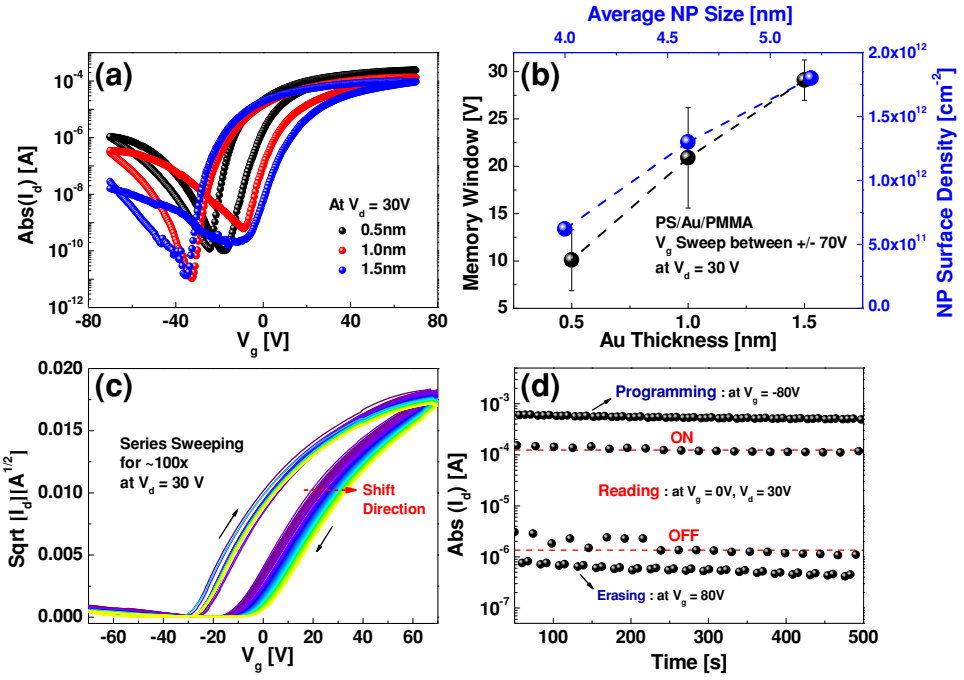

Figure 7. a) Memory hysteresis loops and b) the corresponding memory windows which depended on the thickness of thermally deposited Au NPs. The transfer plots were obtained by V_g sweeps from −80 V to +80 V in the forward and reverse directions at V_d = 30 V. c) Series V_g sweeps made more than 100 times at V_d = 30 V, between ±70 V and d) evolution of the ON and OFF states by the sequential application of programming (at V_g = −80 V and V_d = 0 V), reading (at V_g = 0 V and V_d = 30 V), and erasing (at V_g = +80 V and V_d = 0 V) biases, in the case of the devices with the PS/PMMA dielectric bilayer having Au NPs (1.0 nm).

reading/erasing/reading operations should yield reproducible results. Figure 7c shows the transfer plots for P(NDI2OD-T2)-based OFETs fabricated using NFGs (and whose structure was PS/Au NPs (1.0 nm)/PMMA) during sequential V_g sweeps of ±70 V at V_d = 30 V for more than 100 cycles. The plots show that the clockwise hysteresis loops were stable and remained so even after a number of V_g sweeps. However, the value of V_{Th} during the reverse V_g sweeps increased steadily by ≈10 V, while the onset voltage (V_{on}) for the forward V_g sweeps was ≈−25 V in most cases. It is likely that during the sequential erasing processes, the holes trapped in the NFGs were progressively removed till none of them remained, by either by being released or by being compensated for by oppositely charged charge carriers (i.e., electrons) supplied by the application of a V_g of 70 V. It should be noted that this assumption is speculative, and further investigation into the cause is underway. The Au-NPs-based memory devices were tested by switching them quickly between the high- and low-conductivity states more than 100 times. These NFGM devices, which had an embedded layer of Au NPs 1.0 nm thick, were sequentially programmed, read, and erased, as shown in Figure 7d, with the ON and OFF states being determined by the application of programming (at V_g = −80 V and V_d = 30 V), reading (at V_g = 0 V and V_d = 30 V), and erasing (at V_g = +80 V and V_d = 30 V) biases. The on current I_{on} (logically "1") and off current I_{off} (logically "0") were on the order of 10^{-4} A and 10^{-6} A, respectively, and switching between the two occurred quickly, within ≈0.1 s. This result suggested that the organic NFGMs fabricated by us exhibited reproducible and reversible switching characteristics, with no deterioration being noticed in the on and off currents.

Lastly, we investigated how uniform the performance of the P(NDI2OD-T2)-based NFGMs was. As shown in **Figure 9**a,b,

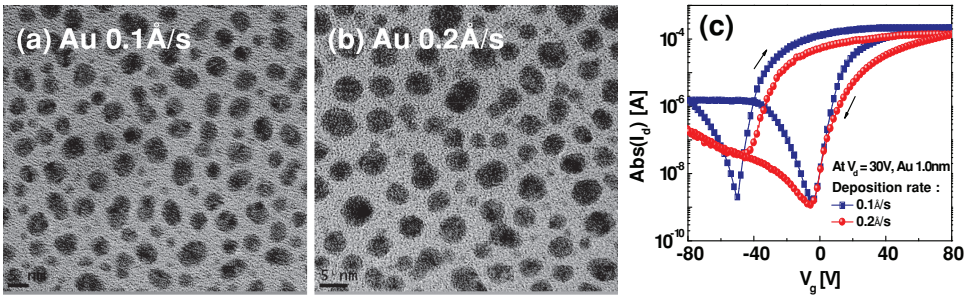

Figure 8. a,b) TEM images of the thermally deposited Au NPs (1.0 nm thick) deposited at different rates: a) at 0.1 Ås^{-1} and b) 0.2 Ås^{-1}. c) Bias hysteresis in the transfer plots, Abs(I_d) vs. V_g at V_d = 30 V, of the OFETs with the Au NPs deposited at different rates: 0.1 Å s^{-1} and 0.2 Å s^{-1}.

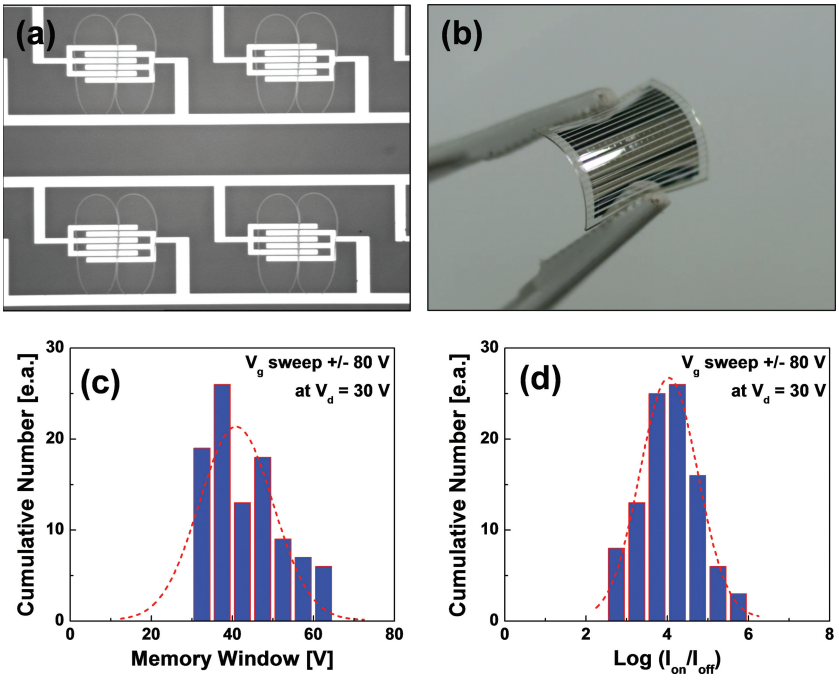

Figure 9. Inkjet-printed and flexible organic NFGM arrays (16 × 16 OFETs, 256-bit). a) A CCD camera image of the active features of an inkjet-printed P(NDI2OD-T2)-based device and b) digital image of the corresponding 256-bit OFET memory array on a flexible PEN substrate. Frequency distributions of the measured values of the c) memory window and d) log(I_{on}/I_{off}) at V_d = 30 V of the devices in the 256-bit memory array on a PEN flexible substrate.

the active layers of P(NDI2OD-T2) were patterned by inkjet printing, and an array of 256-bit (16 × 16 transistors) flexible NFGM devices was fabricated on a PEN substrate. Each of these flexible Au-NPs-based memory cells with the thickness of the layer of Au NPs being 1.0 nm exhibited non-volatile memory characteristics similar to those of the devices fabricated on a glass substrate. The frequency distributions of the memory devices exhibiting various memory windows and I_{on}/I_{off} are shown in Figure 9c,d, respectively. Taking almost 100 memory devices into consideration, the average (standard deviation) memory window and I_{on}/I_{off} were ≈43.5 V (±8.3 V) and ≈10^4 (±$10^{0.85}$), respectively. Moreover, a device yield of more than 99% was achieved, with the deterioration failures associated with FET memory devices not being noticed. Thus, it could be surmised that high-performance organic NFGM devices having layers of metallic NPs (such as those of Au, Ag, or Cu) embedded in them were fabricated successively on a flexible substrate and that they exhibited relatively uniform characteristics.

3. Conclusions

We investigated the effects of using metallic NPs and blocking polymer dielectrics on the characteristics of organic NFGMs fabricated using the high-performance n-type (potentially ambipolar) polymer semiconductor P(NDI2OD-T2) and NPs of various metals (Au, Ag, Cu, and Al) that were embedded within bilayers of different polymer dielectrics (PS/PVP and PS/PMMA). It was found that the characteristics of these NFGM devices depended strongly on the blocking dielectrics (PVP or PMMA) and the NFGs (NPs of Au, Ag, Cu, or Al) used. The NFGM devices with the layer of the blocking dielectric PMMA showed extrapolated retention times longer than those of the PVP-based devices. This was due to the charge relaxation time of PMMA being relatively longer. Interestingly, the NFGM devices fabricated using small- and uniform-sized Au NPs showed the widest memory windows, while the NFGM devices formed using spatially well-distributed Cu NPs exhibited quasi-permanent retention characteristics. The best performing P(NDI2OD-T2)-based NFGM devices, which were the ones fabricated using PMMA and Au NPs, showed excellent memory-related characteristics along with a wide memory window (≈52 V), a high I_{on}/I_{off} (≈10^5), and a long retention time (>10^7 s). We also successfully fabricated an array of 256-bit flexible printed organic NFGMs on a PEN substrate. These optimized flexible memory devices exhibited high I_{on}/I_{off}, wide memory windows, and a high degree of reliability, as measured over 100 devices.

4. Experimental Section

Fabrication of the Organic Field-Effect Transistor (OFET) Memory Devices: The Corning Eagle 2000 glass and polyethylene naphthalate (PEN) (Tenjin DuPont Films) substrates used to fabricate the devices were cleaned with deionized water, acetone, and isopropanol in an ultrasonic cleaner for 10 min each. The adhesion layer, which was 3 nm thick and of nickel, and the Au source/drain (S/D) electrodes (12 nm thick) were patterned on the substrates by conventional photolithography and lift-off processes. The channel width/length (W/L) was 1.0 mm/10 μm. The semiconducting polymer P(NDI2OD-T2) (ActivInk N2200, purchased from Polyera Corp.), having a concentration of ≈10 mg/mL in p-Xylene, was spin coated or inkjet-printed onto the as-cleaned substrates that had the BC Au S/D electrodes. Both the first dielectric layer, i.e., that of PS (concentration of ≈10 mg/mL in n-butyl acetate (nBA)) and the second dielectric layer, i.e., that of PMMA or PVP (concentration of 40–60 mg/mL in 2-ethoxyethanol (2E)) were sequentially spin coated on top of the semiconductor films. All dielectric materials and solvents were purchased from Sigma-Aldrich and used as received. The solutions were filtered through a 0.45 μm polytetrafluoroethylene filter before use. The metallic NPs were deposited by vacuum thermal evaporation on top of the first dielectric layer at a deposition rate of 0.1–0.2 Å/s. The choice of solvents for the dielectrics is critical and was limited to a few orthogonal solvents, in order to prevent the dissolution of the underlying semiconductor and dielectric layers during the process of coating the upper gate dielectric layer.[35] For instance, P(NDI2OD-T2) is insoluble in nBA but PS is, and both PMMA and PVP dissolve in the solvent 2E but PS does not. The semiconductor and dielectric films were thermally annealed at 110 °C and 80 °C for 30 min, respectively. The devices were completed after the vapour deposition of aluminum (Al) gate electrodes (≈35 nm thick) through a metal shadow mask.

Thin Film and Device Characterization: The current-voltage (*IV*) characteristics of the OFET transistors and nonvolatile memory devices based on P(NDI2OD-T2) were measured in a nitrogen-filled glove

box using a Keithley 4200 semiconductor characterization system. Field-emission transmission electron microscopy (FE-TEM) and high-resolution scanning transmission electron microscopy (SEM) combined with energy-dispersive spectroscopy (STEM-EDS), performed using a JEM2200FS transmission electron microscope with an accelerating voltage of 200 kV and a point-to-point resolution of 0.1 nm were used to image the devices. The thicknesses of the thin films were measured using an XP-1 surface profiling system (Ambios Technology, Inc.).

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